REMARKS

Claims 1-8, 10-14, 16-26, 28-29, 31-37, 40-41, 43-46, 48-49, 51-55, 57-60, 77, and 82-106 are currently pending in the application. Of these claims, claims 1, 8, 21, 26, 28, 40, 46, 52, 55, and 58 are independent.

Prior Amendment to Claim 40

Applicant notes claim 40 was previously amended in the Response mailed August 13, 2003 to replace "including" with "capable of" among other amendments. The addition of "capable of", however, was done without underlining. Applicant hereby affirms that "capable of" was to be added to claim 40.

Prior Art Rejections

In the Office Action, claims 1-37 and 40-84 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,860,083 to Sukegawa ("Sukegawa") in view of IBM Technical Disclosure Bulletin NN9411421 ("TDB").

Applicant respectfully traverses these rejections as follows.

Claims 9, 15, 27, 30, 42, 47, 50, 56, 61-76, and 78-81 have been canceled without prejudice or disclaimer. Accordingly, the rejection of these claims is no longer applicable.

Independent claim 1 recites a memory controller operable to execute a queued memory request when a hard disk is accessed in response to a read memory request.

Independent claim 8 recites performing a queued disk memory operation in response to a request for a memory read operation.

Independent claim 21 recites performing a queued disk memory operation in response to a disk read operation.

Independent claim 26 recites queuing a disk write operation to transfer data from a non-volatile cache to a disk in response to a read operation.

Independent claim 28 recites a controller to execute a queued memory request when a storage device is accessed in response to a read request.

Independent claim 40 recites completing queued access requests in response to a read request.

Independent claim 46 recites servicing a queued access request in response to receiving a read request.

Independent claim 52 recites writing data from a non-volatile cache memory to store in a disk memory in response to a cache read miss.

Independent claim 55 recites writing data from a cache memory to a disk memory in response to a cache read miss.

Independent claim 58 recites writing data associated with a write request to a disk memory in response to a cache read miss.

Applicant respectfully submits neither Sukegawa nor TDB, whether alone or in any combination with one another, taught or suggested such features as claimed.

The Office Action states on page 3 at lines 3-8:

> Sukegawa's memory controller determines if a memory request can be satisfied by accessing the cache memory as claimed. * * * If it cannot be satisfied by the cache (such as when a write misses the cache), then it is queued up and executed when the hard disk drive is accessed as claimed (see Sukegawa column 10, lines 5-17).

The Office Action also states on page 6 at lines 8-12:

> What [Sukegawa] doesn't say but what is readily apparent is that once certain access requests (such as reads) are received that cannot be satisfied from the flash memory, the hard disk must be spun up to satisfy the requests. What is obvious is that once the disk is then spun up, the queued requests can quickly and efficiently be "unqueued" or sent to the disk, completing them as claimed.

Applicant respectfully submits, however, that this interpretation of Sukegawa is contradicted by Sukegawa in column 10 at lines 5-17:

> A first modification of the third embodiment relates to a system wherein the non-volatile cache area 10C is provided in advance with a storage area for new data write. According to this system, updated data can be stored in the storage area for new data write, without accessing the HDD 2. Needless to say, updated data has been stored in all the storage area for new data write, the HDD 2 is accessed and the saving process is performed. *In this case, after a certain amount of accumulated updated data is saved in the non-volatile cache area 10C, the HDD 2 is accessed.* As a result, the frequency of access to the HDD 2 is reduced. Because of the reduced frequency of access to the HDD

2, the power can be saved and a silent environment can be achieved. Furthermore, the operation environment of the user can be improved by enabling the user to set the storage area for new data write.

Sukegawa specifically taught updated data in non-volatile cache area 10C is updated to HDD 2 "after a certain amount of accumulated updated data is saved in the non-volatile cache area 10C".

Applicant respectfully requests the identification of specific teachings in Sukegawa to support any interpretation that updated data in non-volatile cache area 10C is updated to HDD 2 in response to a read request, read operation, or cache read miss as claimed by Applicant.

Noting the remaining rejected claims depend from independent claim 1, 8, 21, 28, 40, 46, 52, 55, or 58, Applicant therefore respectfully submits these rejections have been overcome and should accordingly be withdrawn.

Note that there may be additional reasons for the patentability of claims. For example, there may be additional reasons why the dependent claims are patentable.

New Claims

New claims 85-106 depend from independent claim 1, 8, 21, 26, 28, 40, or 46. Applicant therefore respectfully submits new claims 85-106 are also patentable over Sukegawa and TDB. Note that there may be additional reasons for the patentability of these new claims.

It is respectfully submitted this patent application is in condition for allowance, for which early action is earnestly solicited.

The Examiner is invited to telephone the undersigned to help expedite the prosecution of this patent application.

Respectfully submitted,

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